IN THE CLAIMS

Please amend the claims as follows.

1.   (Previously Amended) A method for creating a wire load model, comprising:

creating an interconnect configuration;

running a field solver to generate parasitic information for the interconnect

configuration;

storing the parasitic information in an accessible format, wherein the

parasitic information comprises capacitance and resistance

information; and

running a curve-fitting engine to create the wire load model, wherein

running the curve-fitting engine is dependent on the parasitic

information.

2.   (Original) The method of claim 1, wherein a range of widths and spacings for the

interconnect configuration are chosen so that widths and spacings are larger than a

minimum width and spacing specification for the interconnect configuration.

3.   (Currently Amended) The method of claim ~~1~~2, wherein the accessible format is a

look-up table for the range.

4.   (Original) The method of claim 1, wherein the curve-fitting engine is a non-linear

curve-fitting engine.

5.   (Original) The method of claim 1, wherein the parasitic information comprises at

least one selected from the group consisting of an area capacitance, a coupling

capacitance, and a fringe capacitance.

6.   (Previously Amended) A program storage device readable by a machine, tangibly

embodying a program of instructions executable by the machine to perform a

method for creating a wire load model, the method comprising:

creating a wire structure;

running a field solver to generate parasitic information for the wire

structure, wherein the parasitic information comprises capacitance

and resistance information;

storing the parasitic information in an accessible format; and

running a curve-fitting engine to create the wire load model, wherein

running the curve-fitting engine is dependent on the parasitic

information.

7.   (Original) The method of claim 6, wherein a width and a spacing for the wire

structure is chosen so that the width and spacing is larger than a minimum width

and spacing specification for the wire structure.

8.   (Original) The method of claim 6, wherein the accessible format is a look-up

table.

9.   (Original) The method of claim 6, wherein the curve-fitting engine is a non-linear curve-fitting engine with an error control mechanism.

10.   (Original) The method of claim 6, wherein the parasitic information comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance.

11.   (Previously Amended) A computer system, comprising:

a memory for storing a model of a circuit;

a processor for creating a wire load model, wherein the processor establishes an interconnect configuration for the circuit;

a field solver for determining parasitic information for the interconnect configuration, wherein the parasitic information comprises capacitance and resistance information; and

a curve-fitting engine that uses the parasitic information to generate the wire load model.

12.   (Previously Amended) The computer system of claim 11, wherein a width and a spacing for the interconnect configuration is chosen so that the width and spacing is larger than a minimum width and spacing specification for the interconnect configuration.

13.   (Previously Amended) The computer system of claim 11, wherein the curve-

fitting engine is a non-linear curve-fitting engine.

14.   (Previously Amended) The computer system of claim 11, wherein the parasitic information comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance.

15.   (Previously Amended) A method for creating a wire load model, comprising:

creating an interconnect configuration;

generating parasitic information for the interconnect configuration, wherein the parasitic information comprises capacitance and resistance information;

storing the parasitic information in an accessible format; and

creating the wire load model dependent on the parasitic information.

16.   (Original) The method of claim 15, wherein generating parasitic information uses a field solver.

17.   (Original) The method of claim 15, wherein creating the wire load model uses a non-linear curve-fitting engine.

18.   (Original) The method of claim 15, wherein the parasitic information comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance.

19.   (Previously Amended) A wire load model creation tool, comprising:

    means for creating an interconnection configuration for a structure;

    means for field solving the interconnect configuration to determine parasitic information, wherein the parasitic information comprises capacitance and resistance information;

    means for storing the parasitic information;

    curve-fitting means for curve-fitting the parasitic information and using interconnect configuration parameters to create a wire load model; and

    means for controlling error in the curve-fitting means.

20.   (Previously Added) The method of claim 1, wherein the interconnect configuration is non-symmetrical.

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